REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add one vendor, CAGE 65786. Add device types 03 and 04. Add margin test, programming procedure, waveform, and flowchart for method B. Add case outline letter K.	88-10-25	M. A. Frye
B	Add "Changes in accordance with NOR 5962-R103-92."	91-12-24	M. A. Frye
C	Redraw with changes. Add device type 05 for vendor CAGE number 65786. Changes to margin test methods A and B. Add vendor CAGE number 66579 as a source of supply for device types 01JX, 01LX, and 013X with vendor similar part number changes. Editorial changes throughout.	93-02-23	M. A. Frye

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV																				
SHEET																				

REV STATUS OF SHEETS															
REV	C	C	C	C	C	A	C	C	A	C	C	C	C		
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13		

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Rick Officer

CHECKED BY
Charles Reusing

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
88-01-04

REVISION LEVEL
C

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, MEMORY, DIGITAL, CMOS, 2K X 8 UV ERASABLE PROM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-87650**

SHEET 1 OF 13

DESC FORM 193
JUL 91

5962-E375

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access time
01		2K x 8-bit UVEPROM	50 ns
02		2K x 8-bit UVEPROM	55 ns
03		2K x 8-bit UVEPROM	35 ns
04		2K x 8-bit UVEPROM	45 ns
05		2K x 8-bit UVEPROM	25 ns

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline	Terminals	Package style
J	GDIP1-T24 or CDIP2-T24	24	Dual-in-line
K	GDFP2-F24 or CDFP3-F24	24	Flat pack
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line
3	CQCC1-N28	28	Rectangular leadless chip carrier

1.2.3 Lead finish. The lead finish shall be as specified in MIL-M 38510. flnish letter "X" shall not be marked on the microcircuit or its packaging. The "X" desingnation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC}) . . . . . +4.5 V to +5.5 V
Storage temperature range . . . . . -65°C to +150°C
Voltages on any pin with respect to ground . . . . . -0.6 V to +7.0 V
V_{PP} with respect to ground . . . . . -0.6 V to +14.0 V
Power dissipation (P_D) . . . . . 550 mW 3/
Lead temperature (soldering, 10 seconds) . . . . . +300°C
Thermal resistance, junction-to-case (Θ_{JC}) . . . . . See MIL-STD-1835
Endurance . . . . . 50 cycles/byte, minimum
Data retention . . . . . 10 years, minimum

1.4 Recommended operating conditions.

Case operating temperature range (T_C) . . . . . -55°C to +125°C

1/ Generic numbers are listed on the Standardized Military Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-BUL-103.
2/ Lid shall be transparent to permit ultraviolet light erasure.
3/ Must withstand the added P_D due to short-circuit test; e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuits Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.3.1 Unprogrammed or erased devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B,or C (see 4.3), the devices shall be programmed by the manufacturer prior to test with a checkerboard pattern or equivalent (a minimum of 50 percent of the total number of hits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.2.4 Block diagram. The block diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ 4.5 V dc $\le V_{CC} \le$ 5.5 V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input low voltage	V_{IL}	V_{CC} = 4.5 V and 5.5 V	1,2,3	All	-0.5 2/	0.8	V
Input high voltage	V_{IH}	V_{CC} = 4.5 V and 5.5 V	1,2,3	All	2.0	2/ V_{CC} +0.5	V
Output low voltage 3/	V_{OL}	I_{OL} = 16 mA, V_{CC} = 4.5 V, V_{IL} = 0.8 V, V_{IH} = 2.0 V	1,2,3	All		0.45	V
Output high voltage 3/	V_{OH}	I_{OH} = -4 mA, V_{CC} = 4.5 V, V_{IL} = 0.8 V, V_{IH} = 2.0 V	1,2,3	All	2.4		V
Output short-circuit current 2/	I_{OS}	V_{CC} = 4.5 V and 5.5 V, V_{OUT} = GND	1,2,3	All		200	mA
Input load current 4/	I_{L1}	V_{IN} = 5.5 V and GND	1,2,3	All		±10	µA
Output leakage	I_{LO}	V_{OUT} = 5.5 V and GND	1,2,3	All		±10	µA
Operating current, TTL inputs 5/ 6/ 7/	I_{CC} TTL	$\overline{CS1}$ = V_{IL}, V_{CC} = 5.5 V, O_0 to O_7 = 0 mA, CS2 = CS3 = V_{IH}, addresses cycling between 0 V and 3 V	1,2,3	All		120	mA
Operating current, CMOS inputs 2/ 7/ 8/	I_{CC} CMOS	$\overline{CS1}$ = V_{IL}, V_{CC} = 5.5 V, O_0 to O_7 = 0 mA, CS2 = CS3 = V_{IH}	1,2,3	All		120	mA
Input capacitance	C_{IN}	V_{IN} = 0 V, see 4.3.1c	4	All		10	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V, see 4.3.1c	4	All		12	pF
Address to output delay 9/	t_{ACC}	$\overline{CS1}$ = V_{IL}, CS2 = CS3 = V_{IH}	9,10,11	01		50	ns
				02		55	ns
				03		35	ns
				04		45	ns
				05		25	ns
All chip selects to output delay 9/	t_{CS}	Either $\overline{CS1}$, CS2, or CS3 10/	9,10,11	01, 03,04		25	ns
				02		30	ns
				05		20	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ 4.5 V dc $\le V_{CC} \le$ 5.5 V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
All chip selects high to output float 2/ 9/	t_{DF}	Either $\overline{CS1}$, CS2, or CS3 10/	9,10,11	01,02, 03,04		25	ns
				05		20	ns
Address to output hold 2/ 9/	t_{OH}	$\overline{CS1} = V_{IL}$, CS2 = CS3 = V_{IH}	9,10,11	All	0		ns

1/ All electrical performance characteristics are 100 percent tested unless otherwise noted.
2/ May not be tested, but shall be guaranteed to the limits specified in table I.
3/ These are absolute voltages with respect to device ground pin and include all over shoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4/ Output shall be loaded in accordance with figure 4.
5/ TTL inputs: $V_{IL} \le 0.8$ V, $V_{IH} \ge 2.0$ V.
6/ The frequency equals $1/t_{ACC}$(maximum).
7/ The addresses, (A_0 - A_{10} pins), are toggling between V_{IL} and V_{IH}.
8/ CMOS inputs: V_{IL} = GND ±0.3 V, $V_{IH} = V_{CC}$ ±0.3 V.
9/ See figures 4 and 5.
10/ Worst case of output control signal lines $\overline{CS1}$, CS2, or CS3.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

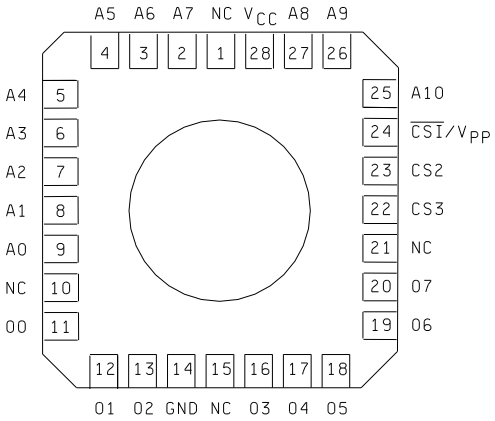
3.10 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.10.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.10.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5.

3.10.3 Verification of erasure of programmability of EPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

Case 3



Cases J, K, and L

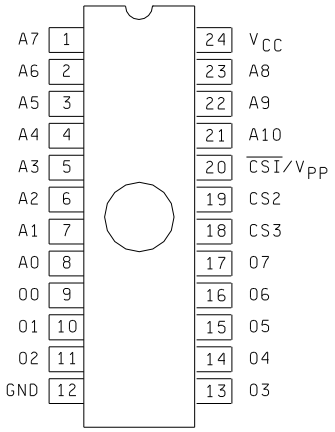


FIGURE 1. Terminal connections.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-87650
		REVISION LEVEL A	SHEET 6

Method A (unprogrammed).

	$\overline{CS1}/V_{PP}$	CS2	CS3	I/O pins
Program	V_{PP}	X	X	Data in
Read	V_{IL}	V_{IH}	V_{IH}	Data out
Deselect	V_{IH}	X	X	High-Z
Deselect	X	V_{IL}	X	High-Z
Deselect	X	X	V_{IL}	High-Z

FIGURE 2. Truth table.

Method B

Pin function					
Mode	Read or output disable	CS3	CS2	$\overline{CS1}$	Outputs
	Other	$\overline{PGM}$	$\overline{VFY}$	V_{PP}	Outputs
Read 1/		V_{IH}	V_{IH}	V_{IL}	Data out
Output disable 1/ 2/		X	X	V_{IH}	High-Z
Output disable 1/ 2/		X	V_{IL}	X	High-Z
Output disable 1/ 2/		V_{IL}	X	X	High-Z
Program 1/		V_{ILP}	V_{IHP}	V_{PP}	Data in
Program verify 1/		V_{IHP}	V_{ILP}	V_{PP}	Data out
Program inhibit 1/		V_{IHP}	V_{IHP}	V_{PP}	High-Z
Intelligent program 1/		V_{ILP}	V_{IHP}	V_{PP}	Data in
Blank check ones 1/		V_{PP}	V_{ILP}	V_{ILP}	Ones
Blank check zeros 1/		V_{PP}	V_{IHP}	V_{ILP}	Zeros

1/ During programming and verification, all unspecified pins to be at V_{ILP}.

2/ X = Don't care but not to exceed V_{CC} plus 5 percent.

FIGURE 2. Truth table - Continued.

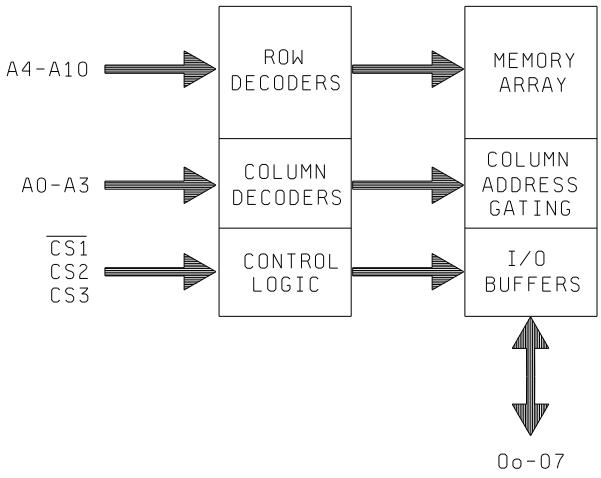
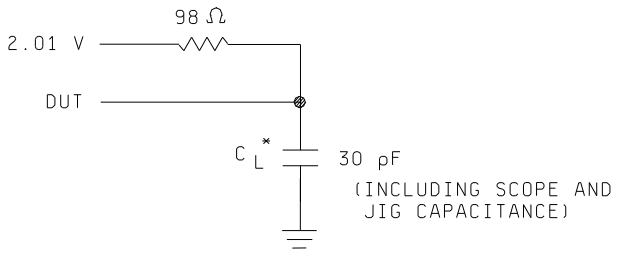


FIGURE 3. Block diagram.

High impedance test systems only



* t_{DF} is tested with C_L = 5 pF.

FIGURE 4. Output load.

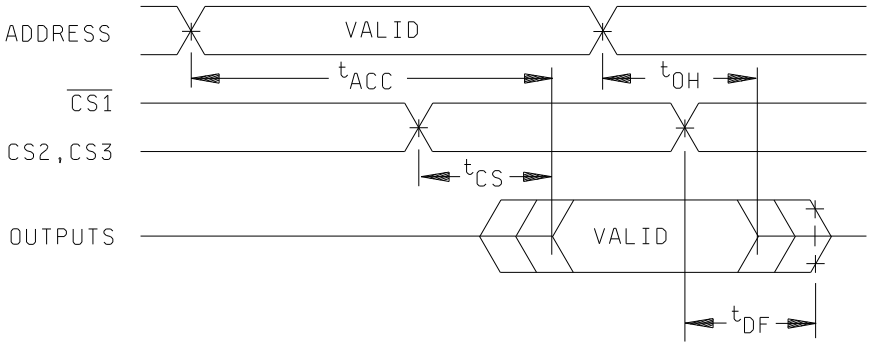


FIGURE 5. AC read timing diagram.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883 .

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. The percent defective allowable (PDA) shall be as specified in MIL-M-38510.

d. A data retention stress shall be included as part of the screening procedure and shall consist of the following steps:

Margin test method A. 4/ (Steps 1 through 5 may be performed at wafer level. The maximum storage temperature shall not exceed +200°C for packaged devices or +300°C for unassembled devices.)

(1) At +25°C, program greater than 95 percent of the bit locations, including the slowest programming cell. The remaining bits shall provide a worse case speed pattern.

(2) Bake unbiased for 72 hours at +140°C or for 48 hours at +150°C or for 8 hours at +200°C, or for unassembled devices only, 72 hours at +225°C.

(3) At +25°C, perform a margin test using V_m = +5.8 V to loose timing (i.e., t_{AA} = 1 µs).

(4) Perform dynamic burn-in in accordance with 4.2a.

(5) At +25°C, perform a margin test using V_m = +5.8 V.

(6) Perform electrical test in accordance with 4.2b.

(7) Repeat steps 5 and 6 at T_C = +125°C and -55°C.

(8) Erase in accordance with 3.10.1. Devices may be submitted to quality conformance inspection.

(9) Verify erasure in accordance with 3.10.3.

Margin test method B. The maximum unbiased bake temperature shall not exceed +200°C for packaged devices or +300°C for unassembled devices.

(1) Program greater than 95 percent of the bit locations, including the slowest programming cell. The remaining cells shall provide a worst case speed pattern.

(2) Bake, unbiased, for 72 hours at +140°C or for 32 hours at +150°C or for 8 hours at +200°C.

(3) Perform margin test using V_M = +4.0 V at +25°C using loose timing, (i.e., t_{ACC} = 1 µs).

(4) Perform dynamic burn-in (see 4.2a).

(5) Perform margin test using V_M = +4.0 V at +25°C.

(6) Perform electrical tests (see 4.2).

4/ Steps 1 through 3 may be performed at wafer level.

(7) Repeat steps 5 and 6 at T_C = +125°C and -55°C.

(8) Erase (see 3.10.1). Device may be submitted for groups A, B, C, and D testing.

(9) Verify erasure (see 3.10.3).

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. Subgroups 7 and 8 shall include verification of the truth table and the EPROM pattern specified in 4.3.1e.

e. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified except for devices being submitted to groups C and D testing.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) The devices selected for testing shall be programmed with a checkerboard pattern. After completion of all listing, the devices shall be erased and verified (except devices submitted for group D testing).

(2) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(3) T_A = +125°C, minimum.

(4) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

c. A reprogrammability test shall be added to group C inspection prior to performing the steady-state life test (see 4.3.2b). The devices to be submitted to the steady-state life testing shall be subjected to the following test and examinations. Each device in the sample shall be subjected to a minimum of 50 program erase cycles.

(1) All devices selected for testing shall be programmed in a checkerboard pattern or equivalent.

(2) Verify pattern (see 3.10.3).

(3) Erase (see 3.10.1).

(4) Verify pattern erasure (see 3.10.3).

4.4 Erasing procedure. The recommended erasure procedure for the device is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for a erasure should be a minimum of 25 Ws/cm^2. The erasure time with this dosage is approximately 35 minutes using an ultraviolet lamp with a 12 mW/cm^2 power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 Ws/cm^2 (1 week at 12 mW/cm^2). Exposure of EPROMS to high intensity UV light for long periods may cause permanent damage.

4.5 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request of the Defense Electronics Supply Center or the original equipment manufacturer, or both.

TABLE II. Electrical test requirements. 1/ 2/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8A, 8B, 9
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8A, 8B

1/ Any or all subgroups may be combined when using high-speed testers.
2/ Subgroups 7 and 8 functional tests shall verify that no cells are programmed for unprogrammed devices or that the altered item drawing pattern exists for programmed devices (see table II).
* Indicates PDA applies to subgroups 1 and 7.
** See 4.3.1c.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 93-02-23

Approved sources of supply for SMD 5962-87650 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-ECS. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-8765001JX	66579	WS57C191-50-DMB
5962-8765001KX	65786	CY7C291-50TMB
5962-8765001LX	66579 65786	WS57C291-50-TMB CY7C291-50WMB
5962-87650013X	66579 65786	WS57C291-50-CMB CY7C291-50QMB
5962-8765002JX	66579	WS57C191-55-DMB
5962-8765002LX	66579	WS57C291-55-TMB
5962-87650023X	66579	WS57C291-55-CMB
5962-8765003KX	65786	CY7C291-35TMB
5962-8765003LX	65786	CY7C291-35WMB
5962-87650033X	65786	CY7C291-35QMB

See footnotes at end of table.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-8765004JX	66579	WS57C191B-45DMB
5962-8765004KX	66579	WS57C291B-45FMB
5962-8765004LX	66579	WS57C291B-45TMB
5962-87650043X	66579	WS57C291B-45CMB
5962-8765005KX	65786	CY7C291A-25TMB
5962-8765005LX	65786	CY7C291A-25WMB
5962-87650053X	65786	CY7C291A-25QMB

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address	Programming procedure letter	Margin test method
65786	Cypress Semiconductor Corporation 3901 North First Street San Jose, CA 95134	B	B
66579	Waferscale Integration, Incorporated 47280 Kato Road Fremont, CA 94538	A	A

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.